SGS-THOMSON MICROELECTRONICS

QN101 QUALITY NOTE

IMPROVED PASSIVATION FOR OTP MEMORY PRODUCTS

The CMOS OTP Memory products are part of the overall EPROM upgrade program through which the process and products are being upgraded, both for performance, reliability and to reach smaller die sizes.

The passivation of the CMOS OTP Memory products manufactured in the E5/0.8 µm upgraded products has been improved. The new passivation is composed of three layers, from bottom to top these are:

- Undopped silicon glass (USG) of 5000Å
- Phosphorous silicon glass (PSG 4%) of 8000Å
- Oxynitride (SiON) of 7000Å

MAIN CHARACTERISTICS

The main benefits of this new passivation are

1. Simpler architecture than the previous passivation. This results in a lower defectivity and a better control of the layer thicknesses.
2. The USG layer is a very good and stable barrier against humidity and all kinds of possible contamination. The conformaity of this layer to the underlying morphology is better than the oxynitride layer. This results in better step coverage over the reduced lithographic dimensions of the smaller die sizes - for example over the smaller metal pitch.
3. The PSG layer is used to provide a self planarisation effect.
4. The SiON layer deposited over the planarised PSG layer completely seals the die surface.

The integrity tests performed at the wafer level and on decapped devices have not revealed any defects.

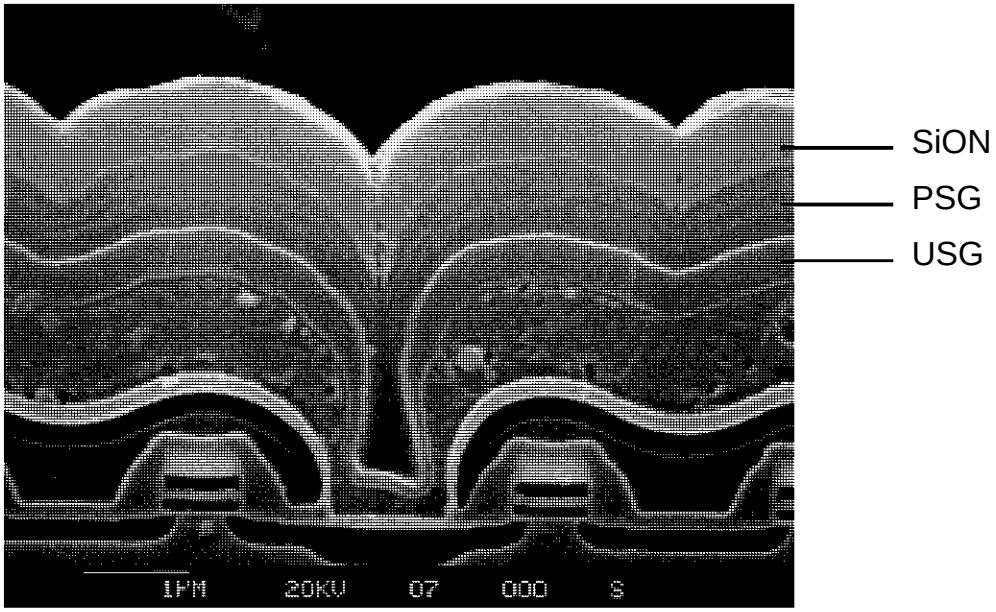
The tables show the results for the 2 Megabit M27C2001 product, made in the CMOS E5/0.8 µm upgrade process technology - with a 10% die size reduction over the original design.

Table 1. M27C2001 - CMOS E5/0.8 micron 10% upgrade, PLCC32 package

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Lots	Fail	Samp.	Note
Operating Life Test	1005	140°C, V_{CC} = 7V, – 168 hrs – 500 hrs – 1000 hrs	 3 3 3	 0 0 0	 180 180 180	
Retention Bake	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs	 3 3 3	 0 0 0	 180 180 180	
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 3 3 3	 0 0 0	 405 405 405	
HAST	CECC 90,000	130°C, RH = 85%, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 1 1 1 1	 0 0 0 0	 32 32 32 32	
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 3 3 3 3	 0 0 0 0	 180 180 180 180	
Temperature Cycling	1010	-65 to 150°C, – 100 cycles – 500 cycles	 3 3	 0 0	 405 405	
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1				

Note: Passivation 0.5µm USG, 0.8µm PSG, 0.7µm SiON

Memory Matrix Area - Polished Cross Section



Flat Area - Polished Cross Section